

## CLAIMS

What is claimed is:

1        1.        A core for providing communications between a transmission media and a  
2        processor in a parallel-serial architecture, said core comprising:

3                serial lanes connecting said processor to said transmission media; and

4                at least one selector connected to said serial lanes, whereby said selector  
5        selectively engages said serial lanes to alter a speed of data passing through said  
6        core.

1        2.        The core in claim 1, further comprising a data controller for controlling an  
2        operation of said selector.

1        3.        The core in claim 1, wherein said serial lanes include buffers for  
2        performing additional speed alteration of said data.

1        4.        The core in claim 3, wherein said buffers comprise elastic first-in, first-out  
2        (FIFO) buffers.

1        5.        The core in claim 1, wherein said selector comprises a multiplexor.

1 6. The core in claim 1, wherein additional speed adjustment is attained by  
2 said selector engaging additional lanes.

1 7. The core in claim 1, wherein said transmission media operates at a  
2 different data speed than said processor.

1 8. A parallel-serial communication system comprising:  
2 at least one processor;  
3 at least one transmission media connecting said at least one processor; and  
4 a core between each processor and said transmission media, said core  
5 providing communications between said transmission media and said, and said  
6 core comprising:  
7 serial lanes connecting said processor to said transmission media; and  
8 at least one selector connected to said serial lanes, whereby said selector  
9 selectively engages said serial lanes to alter a speed of data passing through said  
10 core.

1 9. The parallel-serial communication system in claim 8, further comprising a  
2 data controller for controlling an operation of said selector.

1 10. The parallel-serial communication system in claim 8, wherein said serial  
2 lanes include buffers for performing additional speed alteration of said data.

1 11. The parallel-serial communication system in claim 10, wherein said  
2 buffers comprise elastic first-in, first-out (FIFO) buffers.

1 12. The parallel-serial communication system in claim 8, wherein said selector  
2 comprises a multiplexor.

1 13. The parallel-serial communication system in claim 8, wherein additional  
2 speed adjustment is attained by said selector engaging additional lanes.

1 14. The parallel-serial communication system in claim 8, wherein said  
2 transmission media operates at a different data speed than said processor.

1 15. A core for providing communications between a transmission media and a  
2 processor in a byte-stripped parallel-serial InfiniBand architecture, said core  
3 comprising:  
4 serial lanes connecting said processor to said transmission media; and

5 at least one selector connected to said serial lanes, whereby said selector  
6 selectively engages said serial lanes to alter a speed of data passing through said  
7 core.

1 16. The core in claim 15, further comprising a data controller for controlling  
2 an operation of said selector.

1 17. The core in claim 15, wherein said serial lanes include buffers for  
2 performing additional speed alteration of said data.

1 18. The core in claim 17, wherein said buffers comprise elastic first-in,  
2 first-out (FIFO) buffers.

1 19. The core in claim 15, wherein said selector comprises a multiplexor.

1 20. The core in claim 15, wherein additional speed adjustment is attained by  
2 said selector engaging additional lanes.

1 21. The core in claim 15, wherein said transmission media operates at a  
2 different data speed than said processor.